Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"20020133772"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 20:52
L2	4	"6625785"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 21:14
L3	0	"6625785" and retest	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 20:52
L4	0	"20020133772" and retest	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 20:52
L5	2	"20020133772"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 21:15
L6	2	"6865500"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 21:47
L7	1	10/692586	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 21:53
L8	1	"6865500" and specification and test and alternate and limit$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 21:55
L9	1	"6865500" and specification and test and alternate and limit$3 and boundar$4 and high$3 and low$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 22:16
L10	1	"6865500" and parameter and distribution	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 22:17

L11	1	"6865500" and parameter same distribution	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 22:17
S1	3	test adj4 IC and specificat$5 and guardband	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/12 20:44
S2	3	09/837887	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:12
S3	437	(spec$6 specification) same test same (IC MOS CMOS (integrated adj3 circuit)) same error and test and error	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:14
S4	1	(spec$6 specification) same test same (IC MOS CMOS (integrated adj3 circuit)) same error and test and error and guardband	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:15
S5	41	(spec$6 specification) same test same (IC MOS CMOS (integrated adj3 circuit)) same error and test and error and signature	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:16
S6	14	(spec$6 specification) same test same (IC MOS CMOS (integrated adj3 circuit)) same error and test and error and signature adj4 test	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:23
S7	2554	product same performance same (spec$6 specification) and (CMOS MOS IC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:24
S8	255	product same performance same (spec$6 specification) same test and (CMOS MOS IC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:24
S9	46	product same performance same (spec$6 specification) same test same (CMOS MOS IC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:25

S10	39	product same performance same (spec$6 specification) same test same (CMOS MOS IC) and (threshold$3 bound$6 limit$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/10/15 14:26
S11	26	product same performance same (spec$6 specification) same test same (CMOS MOS IC) and (threshold$3 bound$6 limit$5)	USPAT	OR	ON	2004/10/15 14:57
S12	5	"5748647"	USPAT	OR	ON	2004/10/15 14:48
S13	0	implicit adj3 specification adj3 test$6	USPAT	OR	ON	2004/10/15 14:49
S14	0	test same (limit$4 bound$7 threshold$4) same retest same accept same reject$6	USPAT	OR	ON	2004/10/15 16:49
S15	86	test same (limit$4 bound$7 threshold$4) and retest and accept and reject$6	USPAT	OR	ON	2004/10/15 14:59
S16	18	test same (limit$4 bound$7 threshold$4) and retest and accept and reject$6 and ((integrated adj3 circuit) IC)	USPAT	OR	ON	2004/10/15 15:15
S17	1	IC$3 with test$4 with parameter and alternat$4 adj2 test and pass$3 with fail$4	USPAT	OR	ON	2004/10/15 15:31
S18	2	IC$3 with test$4 with parameter and alternat$4 adj2 test and pass$3 with fail$4	US-PGPUB; USPAT	OR	ON	2004/10/15 16:07
S19	2	("5539652" | "6212667" | "2001/0010091" | "2002/0002698" | "2002/0133772").PN.	USPAT	OR	ON	2004/10/15 15:43
S20	2	IC$3 with test$4 with parameter and alternat$4 adj2 test and pass$3 with fail$4 and specificat$5	US-PGPUB; USPAT	OR	ON	2004/10/15 16:07
S21	47	(test$6 evaluat$4) near4 (limit$4 bound$7 threshold$4) near4 (result$3 signal$2 output$3) and retest$4 and (accep$4 pass$4) and (reject$6 fail$5)	USPAT	OR	ON	2004/10/15 16:52
S22	17	(test$6 evaluat$4) near4 (limit$4 bound$7 threshold$4) near4 (result$3 signal$2 output$3) and retest$4 and (accep$4 pass$4) and (reject$6 fail$5) and (chip IC integrate adj3 circuit)	USPAT	OR	ON	2004/10/15 17:32

S23	0	(test$6 evaluat$4) near4 (limit$4 bound$7 threshold$4) near4 (result$3 signal$2 output$3) and retest$4 and (accep$4 pass$4) and (reject$6 fail$5) and (chip IC integrate adj3 circuit) and alternate	USPAT	OR	ON	2004/10/15 17:33